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Design and Analysis of Low-Power Arithmetic Logic Unit using GDI Technique

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ABSTRACT: The ALU is the most important component of central processing unit and this is also used in microprocessors and embedded systems. In this, ALU consists of full adder , 4bit multiplexer, 2bit and sometimes 8bit multiplexer(if necessary) and is designed to implement logic operations, such as AND, EXOR, EXNOR,OR, etc. and arithmetic operations, as INCREMENT, DECREMENT ADD and SUBTRACT. A design of a 4-bit arithmetic logic unit (ALU) by taking the advantage of the concept of gate diffusion input (GDI) technique. GDI cells are used in the design of full adders and multiplexers which are used to realize ALU. The main objective of the project is to implement an arithmetic logic unit and to reduce the total power of the circuitry by using new technique called GDI(gate diffusion input) Technique. The simulation is carried out in Xilinx and Cadence virtuoso. The Simulation shows that the design is implemented with less power that is 17.08nW and this is very less as compared to 1.122mW (lector technique).
KEYWORDS: Lector, GDI, CPL, TFA, SERF, MTCMOS, Domino Logic, Propagation delay and Power Optimization.

I. INTRODUCTION

In Present era, As the technology is growing more and in terms of IC design, more number of transistors getting packed into an IC, which increases the size and total area in any physical design of device. So, at present, scaling is important for designing any device. So, other than Very large scale integration, there will be a existence of Ultra large scale integration technologies, for faster operation.

For milli to micro, micro to nano and nano to pico regime of structure of new designs existed at present for low-power and high-speed operations. Multiplexer is a Data Selector or digital data switch, where it has 2^n input lines and one (n) output line. The Multiplexer selects required inputs based on the select lines that is, single output is taken from several inputs. The 'n' number of Signals shares one resource, which increases the data rate and passes the input to the output.

Primarily Addition of bits can be achieved by using adders. Further it can be used for complimenting bits and increment and decrement functions etc. But we are concerning about very basic half adder and full adder structures. There is a necessity to build circuit which utilizes low power and with less delay and Faster the operation. Various techniques and topologies have proposed for the same reason. Gate diffusion input is a new Technique of reducing power dissipation, area and delay and achieving high speed and high performance. The combinational circuits also implemented by using this technique. So that, the total circuit area reduction and power reduction is achieved.

II. PREVIOUS WORKS

The Nano CMOS logic also occupies more area and more power but less compared to 28 Transistors. Although still more power and area can be reduced by using complementary transistor logic (CPL) with full adder structured by using 18 transistors and the power consumed here is 2.5uW. A Transmission function full adder (TFA) Technique is a technique of designing of full adder requires 16 transistors and where power consumption is 12uW. One more design technique used is N-cell logic structure of full adder, which utilizes low power and power consumption is 1.67uW. That is a drastic reduction in power can be seen but the output swing is not accurate. Further, Mod2f Full Adder is designed and which requires 14 transistors and utilizes very less area and power. The pass Transistors are used in designing Mod2f Method circuits [1].

The total Optimization of full adder circuit is achieved by 18 transistor dual threshold design. This was the major issue of this technique [2].

The Optimization in area with less power Arithmetic and logic unit is proposed. Where the ALU is implemented by logic gates and pass transistors, where the area optimization is not up to the desired extent. The reduction in Area and power can be achieved by up to 70% as compared to conventional CMOS and as

compared with Transmission gate, it is 30%. In this design, the total area and delay reduction occurs and which in turn reduces the total delay of the circuitry [3].

Pass-transistor logic consists of complementary inputs and outputs and an NMOS pass transistor network. By simply exchanging the input nodes, two inputs AND/NAND, OR/NOR gates or multiplexers can be constructed [4].

Zigzag keeper uses techniques of both sleep transistor and keeper transistor with zigzag approach. Sleep transistors are connected to sleep signal through gate and the gate of keeper transistor are connected to the output of the circuit. During sleep mode, the sleep transistors are turned OFF so preserves the state and prevent any leakage. The keeper transistors are connected to the output of the circuit so during sleep mode they are ON or OFF according to the output to preserve the state. For example if there is high output in second stage then the keeper NMOS transistor will turn ON saving the state of the circuit. In sleep transistor technique the pull-up network and pull-down network are taken of low threshold voltage and sleep transistor is taken of high threshold voltage so in sleep mode sleep transistors will be OFF and as they are of high threshold voltage, they prevent leakage and saves the power [5].

This logic circuit consists of a PMOS load transistor Mp and an NMOS reset transistor Mr and an NMOS block in which inputs are applied. The gates of the load transistor and the reset transistor are connected to clock. When clock =1(reset phase) load transistor Mp is OFF and reset transistor Mr is ON and the output is reset to logic low. Now when clock =0(evaluation phase) load transistor Mp is ON and reset transistor Mr is OFF and the output either goes to logic level high or remains at low logic according to the inputs applied to the NMOS block. So in this output can either go from 0 to 1 or remain at 0 level according to the applied inputs. In FTL the output logic level is evaluated before all the inputs are valid, so its speed is very high [6].

This is a basic approach to reduce the leakage power. MTCMOS reduces the leakage by introducing the high threshold NMOS gating between pull down network and ground terminal, in series to low threshold voltage circuitry. As stated in Dual VT technique is a variation in MTCMOS, in which high threshold voltage can be assigned to transistors of non-critical path to reduce leakage current and low threshold voltage transistors are used in critical paths. An additional mask layer is required due to VT (Threshold voltage) variation, thereby making fabrication process complicated. This technique suffers from latency period i.e. it need some time to get into normal operating mode after reactivation [7].

This modified MTCMOS technique can only reduce the standby leakage power and the introduced MOSFETs results increase in area and delay. During stand-by mode both sleep transistors gets turned off, introducing large resistance in conduction path and thus, leakage current is low. Isolation between VDD and ground path is necessary for leakage reduction. This technique faces a problem for data retention purpose during sleep mode. The Wakeup time and energy of the sleep technique have a significant impact on the efficiency of the circuit [8].

This technique includes duplication of an already present transistor into two half sized transistors. There exists a reverse bias due to duplicated transistors when both the transistors are turned off, which results in sub threshold leakage current reduction. It is a state retention technique with disadvantage of increased delay and area. This technique combines the features of sleepy transistor technique and forced stack technique. In this technique, the sleep transistor is added parallel to the two half sized transistors configuration is used to replace the original transistor in the circuit. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Variation in the width of sleep transistor results tradeoffs in power, area and delay. Additional control and monitoring circuit is required for the sleep transistor [9].

To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique [10].

In LECTOR, the concept of effective stacking transistors has been introduced between the VDD and GND for the leakage power reduction. In this technique two leakage control transistors i.e. P-type and N-type are inserted between the pull up and pull down network of a circuit, in which each LCT gate is controlled by the source of other, hence termed as self-controlled stacked transistors. Since, it is a self-controlled technique so no external circuit is required for controlling purpose. These LCT produces high resistance path between the VDD and GND by turning more than one transistor OFF, thereby reducing the leakage current. This technique has a very low leakage but there is no provision of sleep mode of operation for state retention [11].

Introduction of stacking effect in the circuit results reduction in leakage current flowing across circuit, in GALEOR technique. In this approach, one gate leakage high VT NMOS transistor is introduced between the output and the pull up network and another gated leakage high VT PMOS transistor in inserted between output and the pull down network. Due to the threshold voltage loss caused by high VT MOS transistors, this technique suffers from significant low voltage swing where low logic level appears much above than 0 and high logic level occurs much below than VDD. Increase of propagation delay is result of low output voltage swing [12].

A Low Power Static energy recovery full adder (SERF) is designed. This SERF Full adder is better than DVL adders. This Conventional SERF CMOS Full adder consists of 28 transistors, which consumes more power and more area [13].

The Basic function unit in microprocessors is Arithmetic logic unit. Also using New Methodologies in designing circuits is necessary to reduce power and area. Transmission gates are the gates which use both directions to conduct, for example, like a relay. This transmission gates are used to build full adder circuitry. The Carry is generated by using 2-bit mux and improvement can be seen by power and area Reduction. The design of full adder uses 27 to 18 transistors. Full Adder Circuitry power and area little reduced and performed also increased by using transmission ate to build the full adder circuitry. Here, nano CMOS Technology is used with 20 to 24 transistors used to build full adder structure [14].

The very basic and important component in DSP is Full adders and this is important in microprocessors and microcontrollers also. The main task of full adder is addition but it is used in subtraction and also used in the field of Boolean algebra. The total speed of the system is determined by Adder. So, to reduce power consumption in full adder structure is necessary and also should reduce the threshold problem. To achieve the goal of reducing power, the MOS Transistors are used to reduce power and also to increase the speed. So, 14 transistors are used to build 1 bit full adder circuit. Results noted and which shows an improvement of 50% from threshold loss problem and improvement of 45% in speed. It is far better than SERF structure. The Threshold problem is improved and Power, area also reduced [15].

Static CMOS logic is the most commonly used logic design technique. In this circuit are made up of two networks namely pull up network (PUN) and pull down network (PDN). PUN consists of PMOS transistors and PDN consists of NMOS transistors. Input to these networks is dual of each other. Output is connected to power supply or ground based on the inputs applied to PUN and PDN making the output 1 or 0 respectively. One of the advantages of Static CMOS circuits is that they have high noise margin so they are more scalable than dynamic logic. Therefore threshold voltage of transistors can be lower than dynamic logic circuits. So performance of circuits can be improved which are designed for ultra low voltage. The main drawback of static CMOS logic is that it uses more number of PMOS transistors which increases the delay and area of the circuit. In some consequences, the driving capability of the circuit reduces [16].

An improved version of pass-transistor logic DPL (Double Pass Transistor Logic) is presented. DPL gates consist of both NMOS and PMOS pass transistors, in contrast to CPL gates where only NMOS pass transistors are used. Fullswing operation is obtained by adding the PMOS transistor in parallel with the NMOS transistors. However, this results in increased input capacitance [17].

Domino logic design technique is the improved version of dynamic logic family. Fig. 2 shows domino logic which consists of a dynamic logic circuit followed by a static CMOS inverter. This circuit consists of a PMOS pre-charge transistor MP and an NMOS evaluation transistor MN with their gates connected to clock, and there is an NMOS logic network which implements the required logic function. During the pre-charge phase (Clock = 0) the output of the circuit get charged through the pre-charge transistor MP to the level of VDD and the output of inverter is low. Now during the evaluation phase (Clock =1) the evaluation transistor MN is ON, and the output of the dynamic circuit either discharges to ground or remains at high level depending on the inputs applied to the NMOS network [18].

The pseudo-NMOS logic style is attractive, when designing the complex gates with large fan-ins, because the pull-up network is replaced by a single load transistor Figure. It requires only *N+1* transistors, (where *N* is the fan-in) resulting a smaller area as well as smaller parasitic capacitance. Improved variations of this type of logic style are possible. The first improvement is a simple one with a second large P-MOS pull-up device connected in parallel with the grounded one. This circuit is well suited to a gate that is known to switch only during certain time periods such an address decoder for memory. Recently has been shown that in some circumstances the Pseudo-NMOS logic style could be well suited for low power design. In this paper a new type of a low power full adder cell, S&D full adder that uses Pseudo-NMOS logic style combined with dynamic circuit style is presented [19].

The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). 2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter. The GDI cell structure is different from the existing PTL techniques. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies [20].

III. LECTOR TECHNIQUE

The Low-Power approach introduced before the introduction of GDI Technique is the technique named lector technique, which is the leakage control transistor technique. In this technique, the feedback topology is used. The output leakage is fed back to the input of the circuit, to reduce the current and power consumption. The Figure 1 shows the multiplexer. Where the transistor count seems to be high compared to GDI Technique,

this increases the area and Power consumption. Due to high area necessities there exists a necessity of high wire and wire-length usage so the delay of the circuit increases.

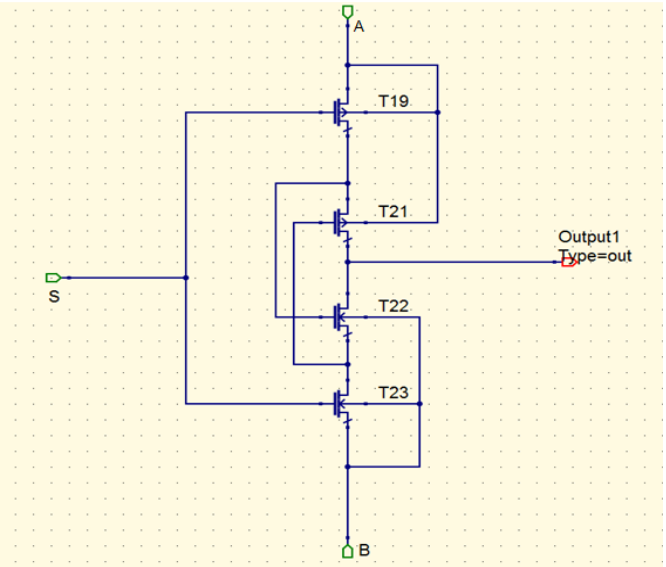


Figure 1 : Lector Based 2-bit Multiplexer

The Figure 2 shows the circuit representation of lector based 4 bit multiplexer. Where the transistor count seems to be very high and as the transistor count increases, which increases the area and which intern increases the power consumption.

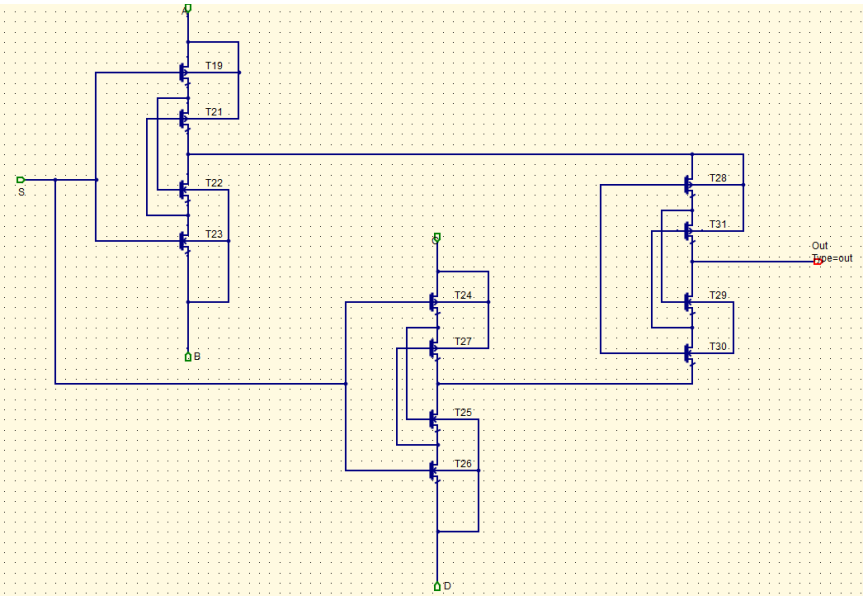


Figure 2 : Lector Based 2-bit Multiplexer

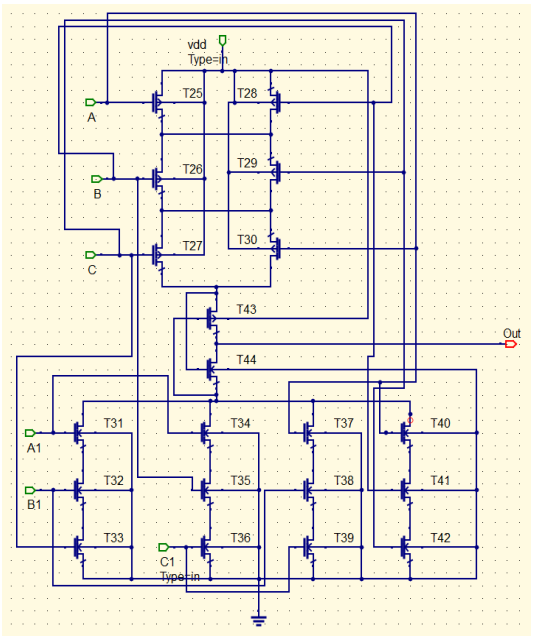


Figure 4 : Lector Based 4- bit ALU

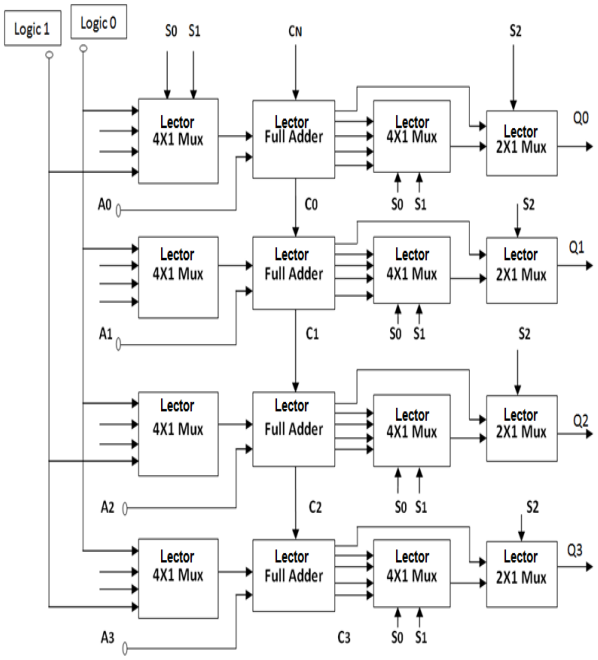


Figure 3 : Lector Based Full Adder

The Figure 3 shows the circuit representation of lector based full adder circuit. Where the transistor count very high compared to GDI and this increases the area and the power consumption.

The Arithmetic operations are necessary and essential in microcontrollers, microprocessors, embedded applications and image and signal processing applications. So, the low power, less delay and less area arithmetic logic circuits are necessary. The Figure 4 shows the circuit representation of lector based full adder circuit. Where the transistor count is high and as the transistor count increases, which increases the area and the power consumption.

IV. GATE DIFFUSION TECHNIQUE

Gate diffusion input is a new Technique of reducing power dissipation, area and delay and achieving high speed and high performance. The combinational circuits also implemented by using this technique. So that, the total circuit area reduction and power reduction is achieved. GDI Technique is a two transistor designing technique, is a two transistor technique, by this the complex logic and arithmetic functions can be determined.

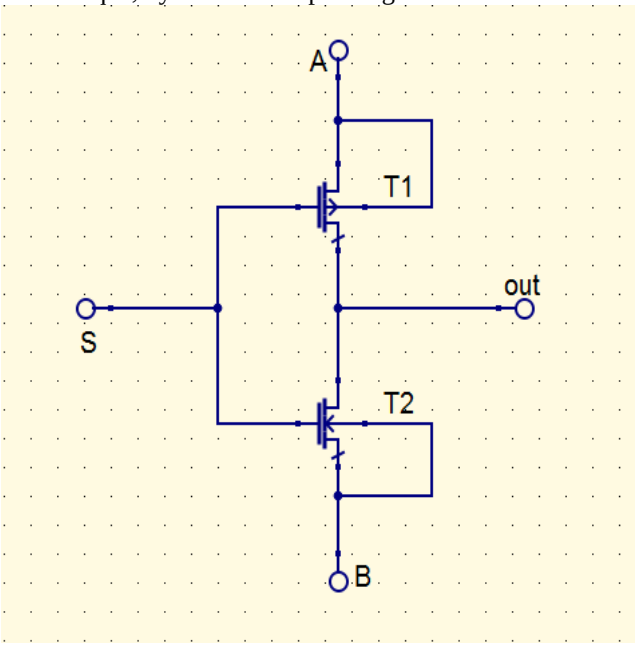


Figure 5 : Basic GDI Cell

GDI Cell is constructed by using three inputs i.e, G (Gate), A (PMOS device source or drain), B (NMOS device source or drain). Where PMOS is not connected to VDD and NMOS is not connected to VSS.

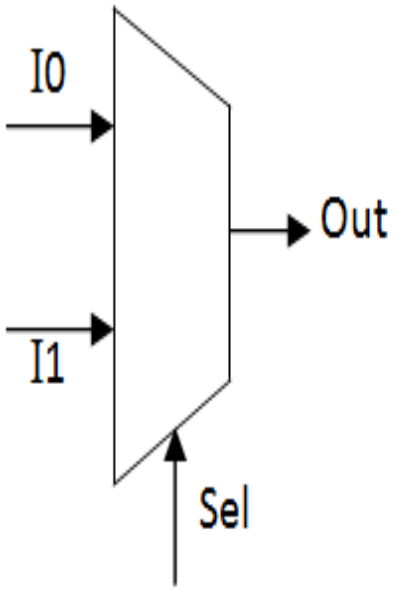


Figure 6 : Block Representation of 2-bit multiplexer

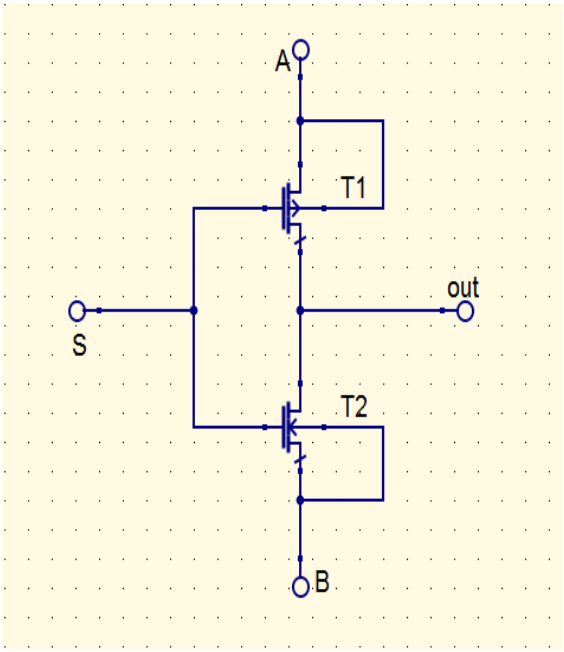


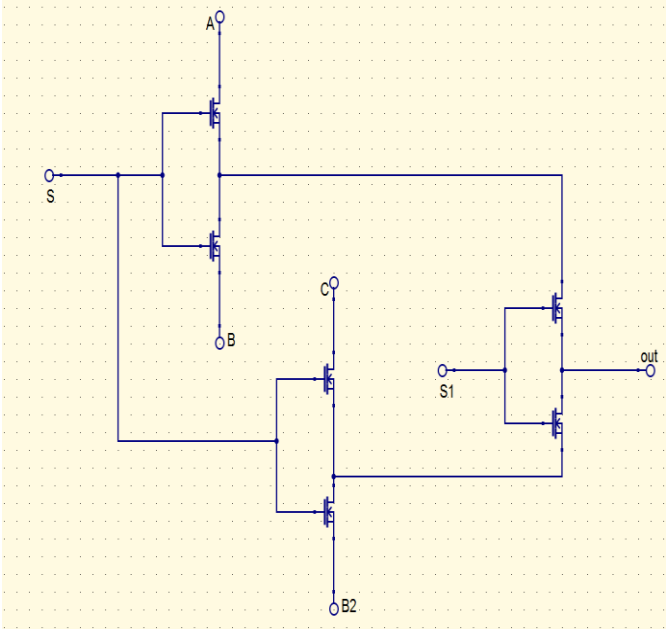
Figure 7 : GDI Circuit Representation of 2-bit multiplexer

Figure 6 and 7 shows the 2 bit multiplexer, where the output is determined by the select lines. Suppose, if select line is zero then I0 input will be getting as output across output. If select line is one, then I1 input will be getting as output across the output terminal.

Table 1 : 2-bit Multiplexer

Select Line	Inputs		Output
Sel	I1	I0	Out
0	0	0	0
1	0	0	0
0	0	1	0
1	0	1	1
0	1	0	1
1	1	0	0
0	1	1	1
1	1	1	1

Figure 8 and 9 shows the 4 bit multiplexer, where the output is determined by the select lines. Suppose, if select lines is zeros then 'A' input will be getting as output across the output terminal. If select lines is '01' then 'B' input will be getting as output, if select lines is '10' then 'C' input will be getting as output and If select lines is all Ones, then D input will be getting as output across the output terminal.



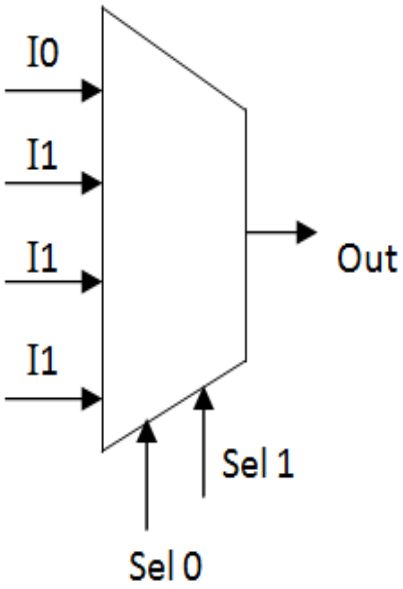
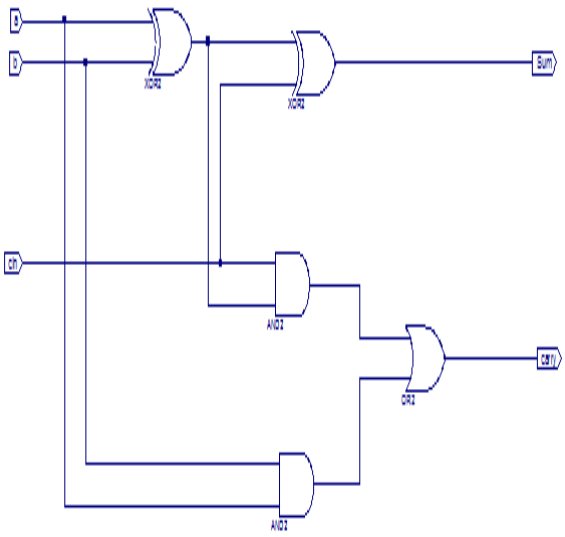


Figure 8 : Block Representation of 4 – bit Multiplexer Figure 9 : Block Representation of 4 – bit Multiplexer

Figure 10 and 11 shows the Full adder circuit constructed using GDI Technique and Table 2 shows the Full adder truth table.



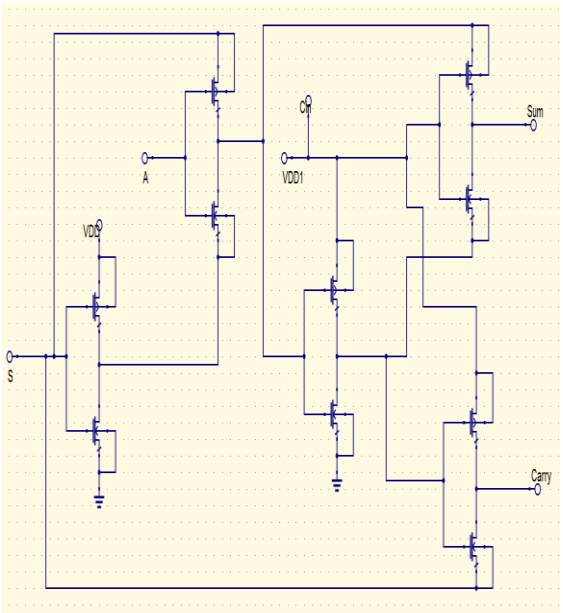


Figure 10 : Boolean Representation of Full Adder Figure 11 : GDI Circuit Representation of Full Adder

Table 2 : Full Adder

Inputs			Outputs	
A	B	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

IV. ARITHMETIC LOGIC UNIT

The Arithmetic Logic circuits are the circuits, in which whose basic operations are addition, subtraction and Boolean operations like, AND, OR and EXOR of bits and increment, decrement etc.., and all this operations are to be performed in a single block, with some changes in condition bits.

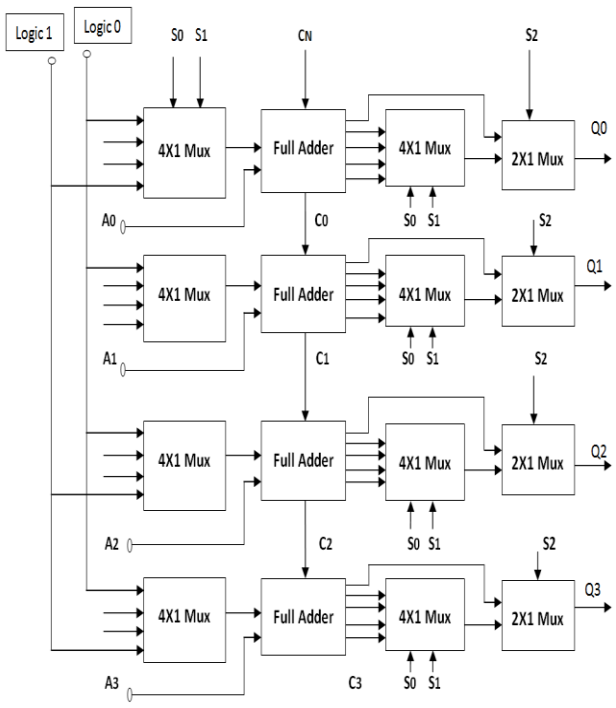


Table 3 : ALU Operations

Selection Lines			Operation
S2	S1	S0	
0	0	0	AND
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBTRACTION
1	1	0	INCREMENT
1	1	1	DECREMENT

Figure 12 : GDI Block representation of 4-Bit ALU

The Increment and decrement operations can be performed by applying logic 1 and logic 0. That is, the increment operation takes place by adding 1 to addend and the decrement operation can be performed by subtraction. For subtraction, the two's complement method is used. The output of full adder is taken as Sum, EXOR, EXNOR, AND and OR, at different points.

The block GDI diagram of 4 bit ALU is shown in Figure 12, based on the condition of the select lines, Full adder computes the results. Table 3 shows the truth table for operations performed by ALU. A Set of S signals that is, S0, S1, and S2 that determines which operation to be selected by ALU. This technique gives better results than previous designs, in terms of power consumption, area and propagation delay.

V. SIMULATION AND OUTPUT ANALYSIS

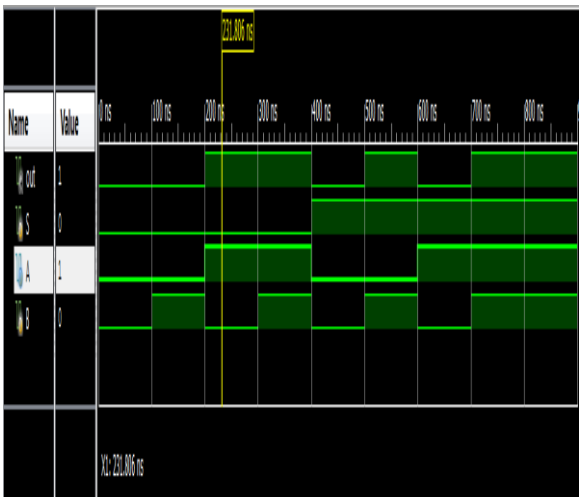


Figure 13 : Simulation of GDI based 2-Bit Multiplexer

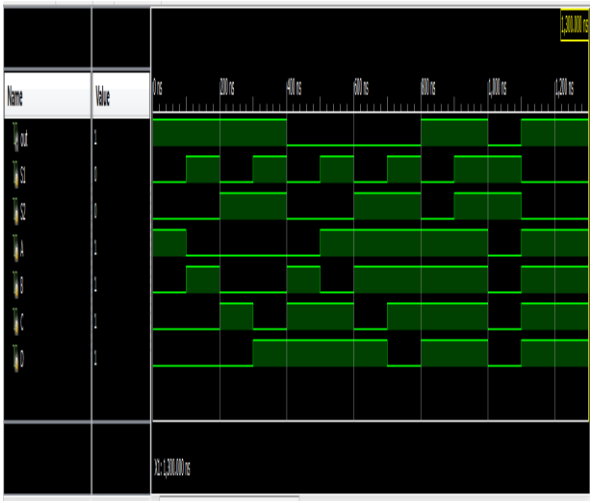


Figure 14 : Simulation of GDI based 4-Bit Multiplexer

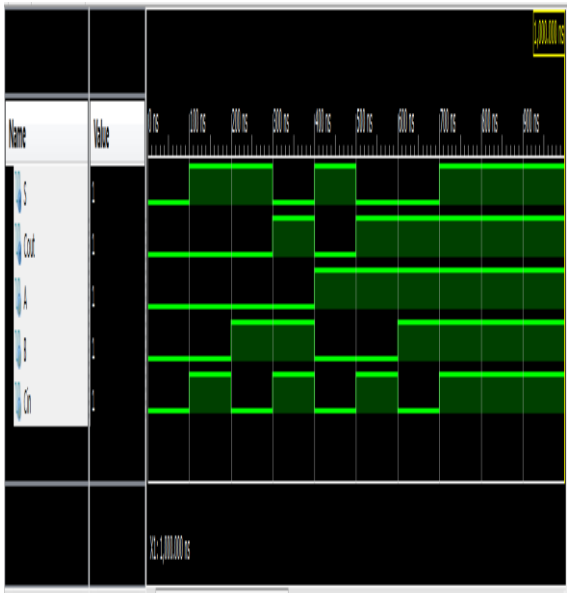


Figure 15 : Simulation of GDI based 4-Bit ALU

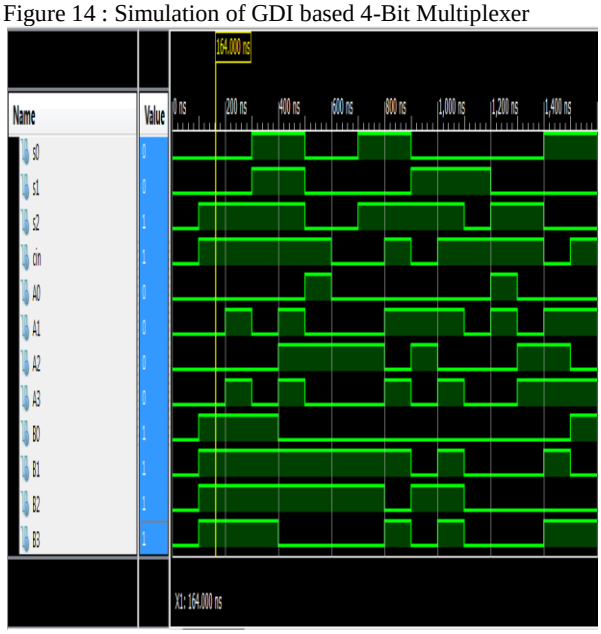


Figure 16 : Simulation of GDI based 4-Bit ALU

Figure 13,14, 15 and 16 shows the simulations of 2-bit, 4-bit multiplexer, full adder and ALU. Power analysis of previous and proposed works and comparisons are estimated as shown in Table 4.

VI. POWER CALCULATIONS

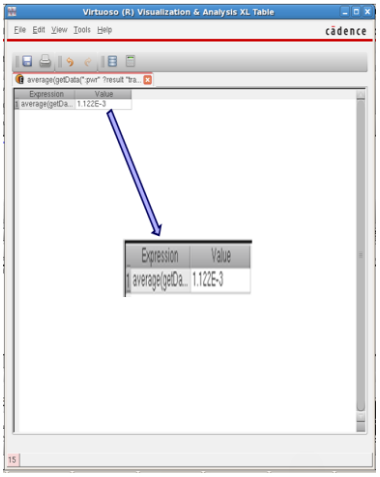


Figure 17 : ALU using Lector technique

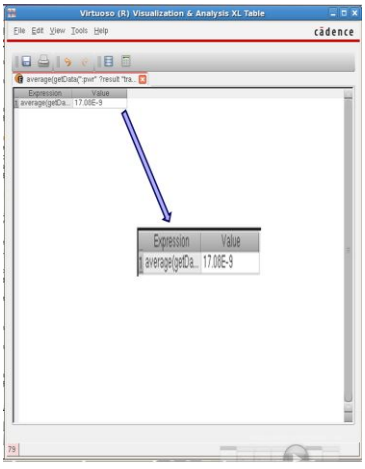


Figure 18 : ALU using GDI technique

The power consumption of ALU's by using lector and GDI technique is as shown in the Figure 17 and Figure 18.

Table 4 : Total Power Consumption

Lector Technique	Power	GDI Technique	Power
2-bit Multiplexer	30.85µW	2-bit Multiplexer	13.8µW
4-bit Multiplexer	25.64µW	4-bit Multiplexer	7.743µW
Full Adder	7.93µW	Full Adder	6.699nW
ALU's	1.122mW	ALU's	17.08nW

Table 4 shows the Power Consumptions of Lector and GDI Technique full adder and ALU. Where we can see that using GDI technique, power is got reduced to maximum. The power consumption of 2-bit multiplexer, 4-bit multiplexer, Full adders and ALU's by using Lector and GDI Technique.

VII. CONCLUSION

The CMOS Circuit Power consumption is increasing as the number transistors increase into a single chip. The static power of the circuit can be neglected but the dynamic power of the affects the total power of the system. This GDI implementation of the circuits reduces the dynamic power of the circuit. A 4-bit ALU is designed and implemented by this technique with low power and in 250nm technology. The multiplexers, full adders are implemented by using this technique with low power and area and these are the main components to build ALU. So the total power and area of the circuit reduces and the delay of the circuit also decreases. This is the best technique as compared to Lector Technique. GDI technique provides best results to the designers. The Simulation shows that the design is implemented with less power that is 17.08nW and this is very less as compared to 1.122mW (lector technique).

VIII. ACKNOWLEDGMENTS

The authors would like to thank the authors of Various Transistor design techniques and various low power circuitry topologies.

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